Remarks

In the present response, three claims (1, 19, and 29) are amended. Applicants believe that no new matter is entered. Claims 1-30 are presented for examination.

I. Claim Rejections: 35 USC § 102

Claims 1-10 and 19-30 are rejected under 35 USC § 102(e) as being anticipated by USPN 6,813,208 to Baker (hereinafter Baker). This rejection is traversed.

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. See MPEP § 2131, also, *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Since Baker neither teaches nor suggests each element in claims 1-10 and 19-30, these claims are allowable over Baker.

Claim 1

Independent claim 1 recites numerous limitations that are not taught or suggested in Baker. For example, claim 1 recites "a read circuit configured to ... obtain a sense result and **adjust the read circuit** based on the sensed result" (emphasis added). By contrast, Baker teaches:

> [Th]e read circuit 300 generates single N-bit count SCNT having a single MSB bit indicating the logic state of data stored in the selected memory cell, as will be explained in more detail below. By eliminating the need to utilize the reference count RCNT and the need to compare two N-bit counts, the data circuit 300 provides a simplified and reliable circuit for reading data from MRAM memory cells. (See col. 5, lines 47-54).

Thus, Baker merely teaches that the read circuit generates a sense count "corresponding to the logic state of the data stored in a selected memory cell" (see col. 5, lines 40-41). Nowhere does Baker teach or suggest that the read circuit obtains a sense result and **adjusts** the read circuit based on a sensed result.

Dependent claims 2-12 depend from claim 1 and thus inherit all the limitations of base claim 1. Thus, for at least the reasons given in connection with claim 1, dependent claims 2-12 are allowable over Baker.

Claim 19

Independent claim 19 recites numerous limitations that are not taught or suggested in Baker. For example, claim 19 recites "an up/down counter that provides a calibration value to **calibrate** a read circuit **to improve reliability of read operations**" (emphasis added). By contrast, Baker teaches an up/down counter that performs a different function. As taught in Baker:

> The UCLK, DCLK signal pulses are applied through a switching circuit 304 to clock and up/down counter 306 which generates an N-bit sense count SCNT in response to the applied signal pulses. The SCNT count of the counter 306 is initially set to an initial value IV, which is thereafter incremented in response to UCLK signal pulses applied to an up input UP of the counter, and is decremented in response to DCLK signal pulses applied to a down input DN of the counter, as will be described in more detail below. (See col. 6, lines 35-43).

Thus, Baker teaches an up/down counter that generates an N-bit sense count SCNT which is thereafter incremented or decremented depending on applied signals. Nowhere does Baker teach or suggest that an up/down counter provides a calibration value to calibrate a read circuit to improve reliability of read operations.

Dependent claims 20-21 depend from claim 19 and thus inherit all the limitations of base claim 19. Thus, for at least the reasons given in connection with claim 19, dependent claims 20-21 are allowable over Baker.

Claim 22

Independent claim 22 recites numerous limitations that are not taught or suggested in Baker. For example, claim 22 recites "clocking an up/down counter **to adjust a calibration value**" (emphasis added).

By contrast, Baker teaches an up/down counter that performs a different function. As taught in Baker:

> The UCLK, DCLK signal pulses are applied through a switching circuit 304 to clock and up/down counter 306 which generates an N-bit sense count SCNT in response to the applied signal pulses. The SCNT count of the counter 306 is initially set to an initial value IV, which is thereafter incremented in response to UCLK signal pulses applied to an up input UP of the counter, and is decremented in response to DCLK signal pulses applied to a down input DN of the counter, as will be described in more detail below. (See col. 6, lines 35-43).

Thus, Baker teaches an up/down counter that generates an N-bit sense count SCNT which is thereafter incremented or decremented depending on applied signals. Nowhere does Baker teach or suggest clocking an up/down counter to adjust a calibration value.

Dependent claims 23-26 depend from claim 22 and thus inherit all the limitations of base claim 22. Thus, for at least the reasons given in connection with claim 22, dependent claims 23-26 are allowable over Baker.

Claim 27

Independent claim 27 recites numerous limitations that are not taught or suggested in Baker. For example, claim 27 recites (emphasis added):

> obtaining a sense result that **represents an integration time for the sense operation;**
>
> comparing the sense result to a threshold value; and
>
> **applying a clock signal to the up/down counter in the event the sense result exceeds the threshold value.**

First, Baker teaches that the read circuit generates a sense count "corresponding to the logic state of the data stored in a selected memory cell" (see col. 5, lines 40-41).

Nowhere does Baker teach or suggest obtaining a sense result that represents an integration time for the sense operation.

Second, Baker teaches an up/down counter that generates an N-bit sense count SCNT which is thereafter incremented or decremented depending on applied signals (see col. 6, lines 35-43). Nowhere does Baker teach or suggest applying a clock signal to the up/down counter in the event the sense result exceeds the threshold value.

Dependent claim 28 depends from claim 27 and thus inherits all the limitations of base claim 27. Thus, for at least the reasons given in connection with claim 27, dependent claim 28 is allowable over Baker.

Claim 29

Independent claim 29 recites numerous limitations that are not taught or suggested in Baker. For example, claim 29 recites numerous elements to calibrate a read circuit in a magnetic memory to improve read operations of the read circuit. Baker teaches that the read circuit generates a sense count "corresponding to the logic state of the data stored in a selected memory cell" (see col. 5, lines 40-41). Nowhere does Baker teach or suggest numerous steps to calibrate a read circuit in a magnetic memory to improve read operations of the read circuit.

Dependent claim 30 depends from claim 29 and thus inherits all the limitations of base claim 29. Thus, for at least the reasons given in connection with claim 29, dependent claim 30 is allowable over Baker.

II. Allowable Subject-Matter

Applicants thank the Examiner for allowing claims 11-18.

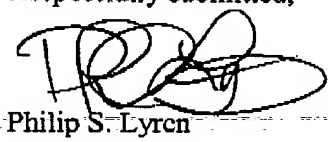
CONCLUSION

In view of the above, Applicants believe all pending claims are in condition for allowance. Allowance of these claims is respectfully requested.

Any inquiry regarding this Amendment and Response should be directed to Philip S. Lyren at Telephone No. (281) 514-8236, Facsimile No. (281) 514-8332. In addition, all correspondence should continue to be directed to the following address:

Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Respectfully submitted,



Philip S. Lyren
Reg. No. 40,709
Ph: 281-514-8236

CERTIFICATE UNDER 37 C.F.R. 1.8

The undersigned hereby certifies that this paper or papers, as described herein, is being transmitted to the United States Patent and Trademark Office facsimile number 703-872-9306 on this 23rd day of February, 2005.

By Be Henry
Name: Be Henry